

### Introduction

The Altera transceivers implement a full XAUI PCS, but only in single-width mode. In single-width mode, the serialization / de-serialization shift registers are 20-bits wide. This limits the XAUI PCS performance to 3.75 Gbps / lane.

The Octera Solutions High Speed XAUI PCS uses the Altera transceivers in double-width mode. The transceivers are used in "basic" double-width mode.

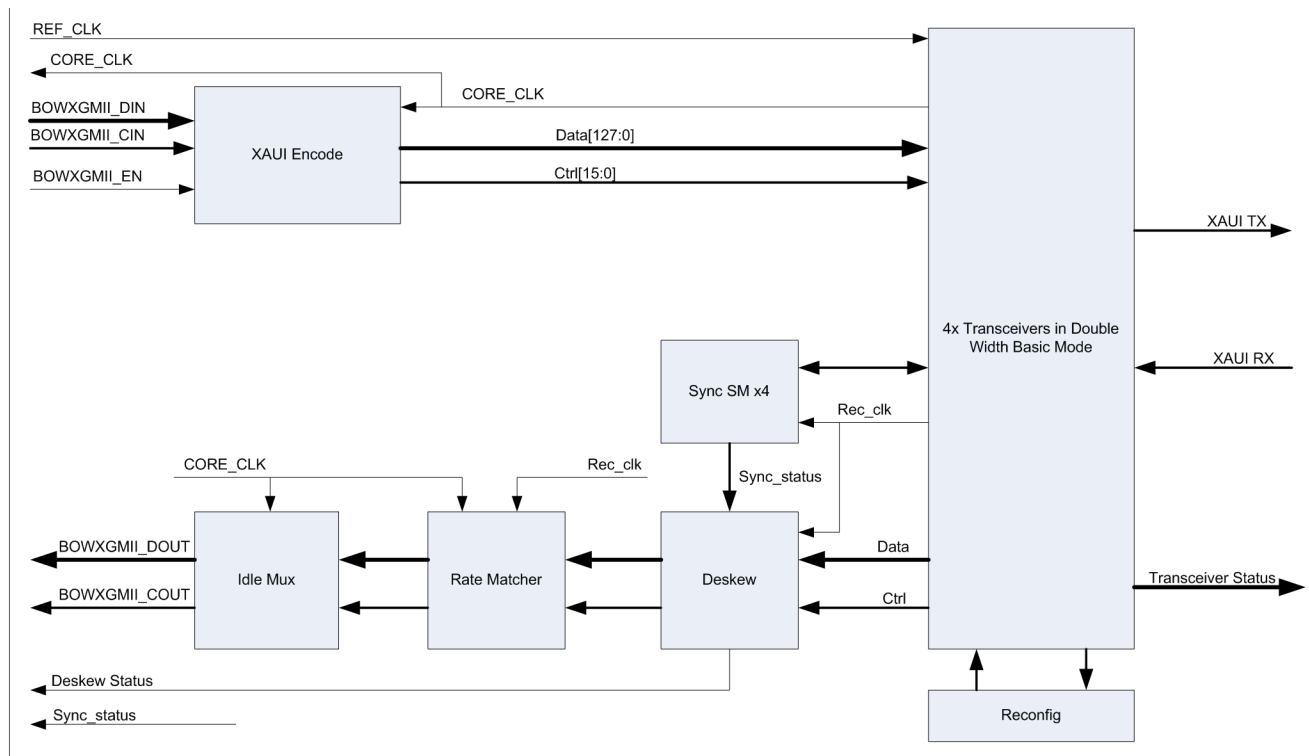
The additional modules required to implement the XAUI PCS are implemented in the FPGA fabric.

The PCS modules are implemented with a data path width of 128-bits, and are efficiently pipelined.

The double-width XAUI PCS operates over the transceiver's usable frequency range.

### Features

- 128-bit Data and 16-bit control MAC interface
- Deskew status, mis-alignment detection, and clock rate sync error bits in addition to transceiver status bits
- IEEE802.3 clause 48-compliant XAUI Idle Encoder
- XAUI Synchronization state machine
- XAUI Lane-to-lane Deskew module
- XAUI Clock rate synchronization
- XAUI Error propagation as 1, 0xFE control character
- Transmit and Receive support reduced minimum average IPG of 8 characters
- PMA Loopback



**Implementation summary**

Core specifics		
Supported	Stratix 4 GX FPGAs	
Resources used		
	Typ	
ALUTs	3,188	
Registers	3,416	
RAM	5,112 bits	
Supported Design Tools		
Altera Tool	Quartus II 9.1 or later	
Speed Grade		
C2 required for high-speed transceivers		
Order code		
OCT-FASTXAUI		

**Customization**

- If required, an Async FIFO for status bits originating in the recovered clock domain can be included.
- If required, expansion from / reduction to a 64-bit data path can be included (applicable to lower speed applications)

**Contact**

Octera Solutions Inc.  
3222 Grey Hawk Court  
Carlsbad, CA 92010

Tel: +1 858 375 4826

Email: sales@octerasolutions.com

www.octerasolutions.com

**Deliverables**

- RTL source in Verilog
- ModelSim wave file (.wlf file) for transmit test with all signals logged
- ModelSim wave file (.wlf file) for receive test with all signals logged
- Full design documentation
- Example Quartus build scripts and TimeQuest constraint file