

Introduction

DDR3 is rapidly becoming the system memory of choice in high volume applications and is therefore the memory standard with the best availability, cost / density and longevity. Standard DDR3 controllers normally operate at 300MHz and above, a higher I/O speed than is available in low cost FPGAs. Octera's DDR3 controller uses the JEDEC standard non-DLL mode of operation to operate DDR3 at 125MHz and is thus available for the low cost Altera Cyclone 3 and Cyclone 4 families.

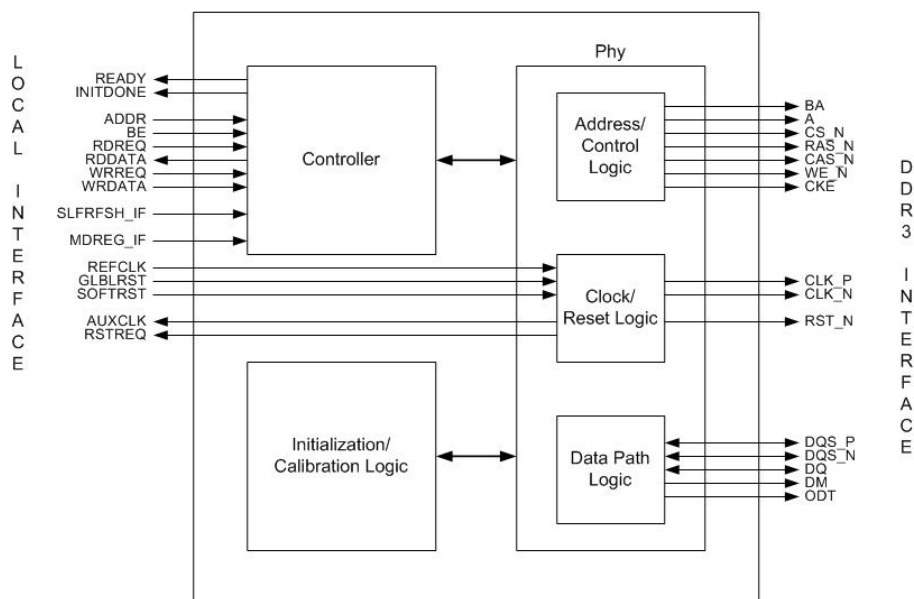
Features

- Variable memory configuration (x4, x8, x16)
- Variable memory burst length
- Both registered and unregistered DIMM
- 8 or 10 precharge address bit number
- Programmable mode register values
- Variable number of column bits

- Variable number of clock outputs
- Variable number of chip select / cke outputs
- Variable number of address bits
- Variable number of bank address bits
- Variable number of strobe bits
- Variable number of data bits
- Variable number of mask bits

Compared to a standard DDR3 controller, Octera's DDR3 core has been designed to allow mode register writes and self-refresh commands prior to the completion of the initialization and calibration sequence and the initialization sequence has been shortened. In addition, the calibration logic has been designed to account for the additional delay introduced by the clock driver on the read data.

Octera DDR3 SDRAM Core



Implementation summary

Core specifics		
Supported	Cyclone 3 and above	
Resources used		
	Typ	
LE's	3021	
Registers	1680	
RAM	1568	
Supported Design Tools		
Altera Tool	Quartus II 9.1 SP1 or later	
Speed Grade		
All		
Order code		
OCT-DDR3-CYCLONE		

Deliverables

- Verilog encrypted source code
- Scripted verification environment
- DDR3 Bus Functional Models

Contact

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