OCTERA Technology Solutions

1588 Timestamping

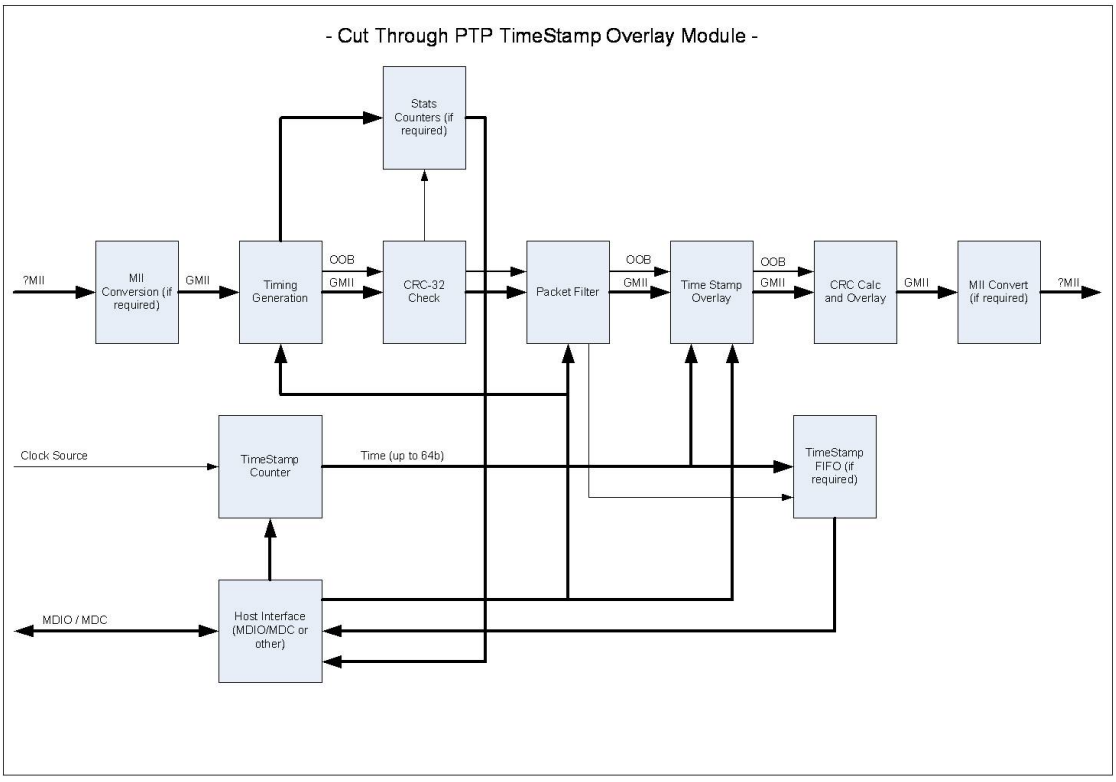
Version 1.2 August 2009

Introduction

The 1588 'industrial' Ethernet standard allows synchronization of time events across multiple devices connected on a single Ethernet network.
A key design component of such synchronization is a time stamping module designed to add time information to Ethernet packets.
Octera provides such a time stamping design as a customizable module for Altera FPGAs. The design can be implemented with on-chip Serdes (Arria and Stratix families) or an external PHY for a low cost (Cyclone) FPGA design. The design can be licensed as source code and Octera offers customization under a design services engagement. The module can be combined with Octera's verification environment (GO-SIM-VER) and Ethernet packet generator module (TGEN) to quickly develop an FPGA providing the time stamping 1588 functionality.
The design consists of multiple modules, not all of which are required depending on the features of the specific design.

1588 timestamp module core features

- Fixed latency cut-through design
- Packets are never de-framed and re-framed, so IPGs are preserved
- No MAC – requires an upstream MAC
- Timer may be asynchronous to data path
- Can support different media independent interfaces
- Can support different host interfaces
- Can support different time stamp sizes
- Can support follow-on time stamping



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Implementation summary

Core specifics		
Supported	Cyclone 3C5 and larger FPGAs	
Resources used		
	Typ	
LE's	3,435	
Registers	2,502	
RAM	33,116	
Supported Design Tools		
Altera Tool	Quartus II 9.0 or later	
Speed Grade		
C8 or faster		
Order code		
OCT-1588		

Customization

The design is offered with multiple optional modules to allow a high level of customization for specific customer requirements. Please contact us to discuss your specific needs, but in general optional modules are:

- Interface modules to convert non-GMII to GMII
- Timestamp FIFO to generate a follow on packet implementation
- Avalon host bus interface defaults to MDIO / MDC but other protocols can be supported

Contact

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Deliverables

- Verilog source code or encrypted source code depending on license
- Scripted verification environment including ethernet traffic
- Optional Ethernet traffic generator and completely flexible verification environment available