

Introduction

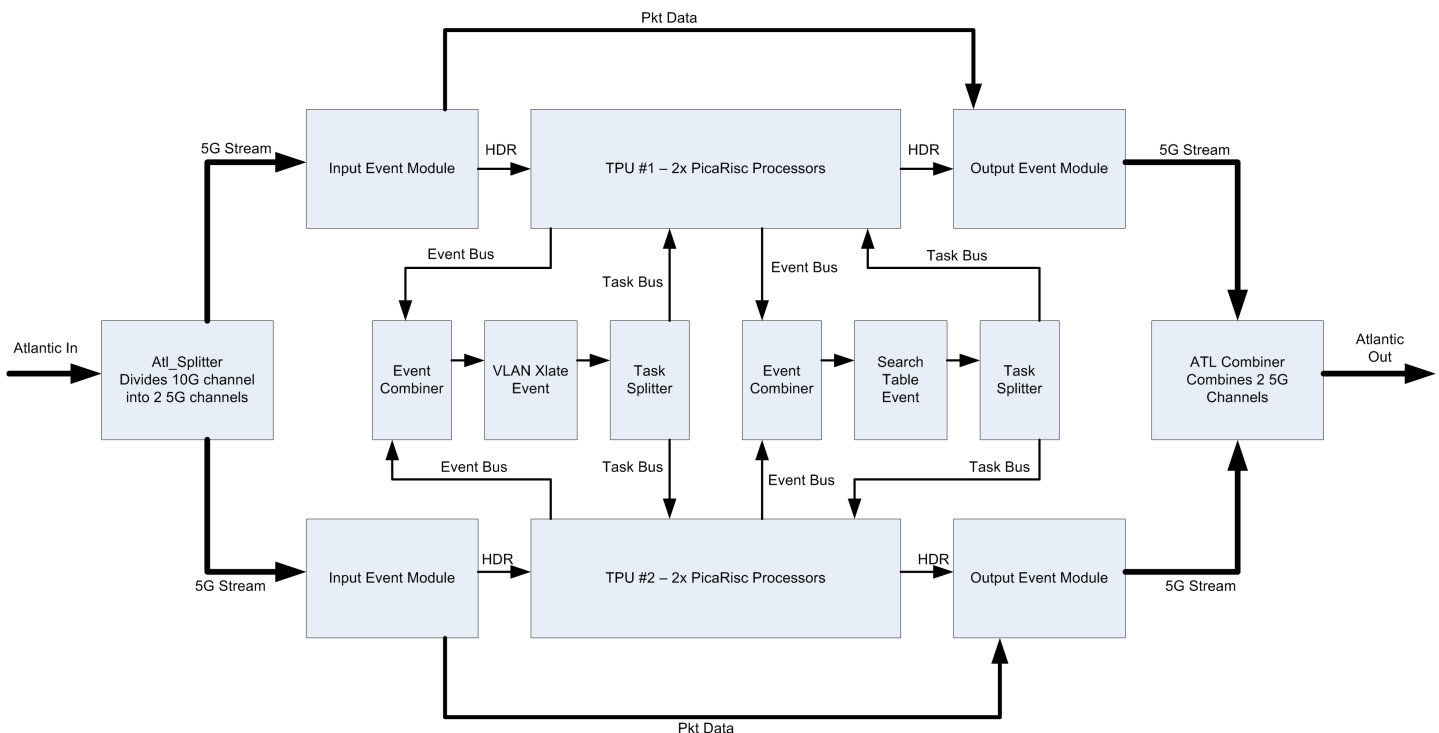
Octera's 10G packet processing reference design is provided as an example of how high speed packet processing can be accomplished in an FPGA using a combination of HW and SW. The processing power is provided by Altera's® multi-core packet processing engine, four of which are instantiated within the design. Each processor core contains eight RISC style processing engines for a total of thirty two processor cores available for SW packet processing.

In addition Octera has added HW acceleration to the design to fully implement the 10G line rate.

Design features

- ATL Splitter
 - Splits 10G Stream into 2 5G streams
 - Packets ping-pong between streams unless one has a FIFO AF condition
 - Generates an 8-bit sequence count for packet re-ordering. Assumes packets are never out of sequence by more than 256

- ATL Combiner
 - Atlantic bus input and output
 - Combines 2 5G streams into a single 10G stream
 - Orders packets based on sequence count
 - Atlantic bus input and output
- TPU Module
 - Instantiates Dual Picarisc TPU
 - Instantiates Avalon + Debug modules
 - Instantiates Monitor module
 - Instantiates Event Bus de-mux
 - Instantiates Task Bus mux
 - Instantiates Input Event Module
 - Instantiates Output Event Module
 - Routes out 2 event busses
 - Routes in 2 task busses



- Event Combiner
 - Accepts 2 Event Busses
 - FIFOs bus requests into separate FIFOs
 - Alternately reads FIFOs and generates single output event bus
- Task Splitter
 - Accepts 1 Task Bus
 - Writes to one of 2 busses based on upper bit of task address
- Event Combiner and Task Splitter allow a single 10G Capable event module to support 2 TPUs

Implementation summary

Core specifics		
Supported	Stratix 2 and higher	
Resources used		
	Typ	
LE's	10,100	
Registers	16,500	
RAM	218 M4K, 3 MRAM, 39 M512	
Supported Design Tools		
Altera Tool	Quartus II 9.0 or later	
Speed Grade		
Any		
Order code		
OCT-10GPACKET		

Contact

Octera Solutions Inc.
3222 Grey Hawk Court
Carlsbad, CA 92010

Tel: +1 858 375 4826

Email: sales@octerasolutions.com

www.octerasolutions.com

Deliverables

- Verilog source code
- Verification environment
 - Includes scripted Ethernet traffic
 - Full Ethernet traffic generator (OCT-TGEN) also available
- Documentation
- Fully supported by Octera field technical personnel and design team